An Altruistic Processor: Update
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AAP Block Diagram

- 4 - 64 Registers
- Code Memories (words)
- Data Memories (bytes)
- ALU
- STATUS/PC

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Current work

- ISA stable
- Code memory width optionally 16/24 bit
  - play with non-power-of-2 units
- Data memory with optionally 8/16/24 bit
  - play with non-octet chars
- AAP patches submitted and reviewed for LLVM
  - need to demonstrate a community
MyStorm Implementation

• “In progress”
  - 16-bit instructions only, 16 registers only
  - UART for debug

• Status
  - compiles and executes on Verilator
    000000: 14 01        ADD     R0, R0, #1
    000001: 41 FF        BRA.s   -1
  - synthesizes for MyStorm using Yosys
  - no memory chip on my board :-(

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promoted 7 nets
1 sr/we
4 cen/wclk/e
2 clk
7 globals
1 sr/we
4 cen/wclk/e
2 clk
realize_constants...
realized 1
place...
initial wire length = 65088
at iteration #50: temp = 10.0458, wire length = 71140
...
at iteration #250: temp = 0.00397257, wire length = 15510
final wire length = 15359
After placement:
PIOs 32 / 107
PLBs 686 / 960
BRAMs 0 / 32

place time 39.63s
route...
pass 1, 254 shared.
...
pass 12, 0 shared.

After routing:
span_4 10264 / 29696
span_12 1649 / 5632

route time 48.31s
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