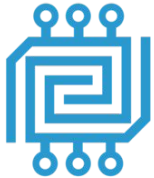
OpenRISC Update

What Happened?

Stafford Horne



ORConf 2023

What is ORConf?

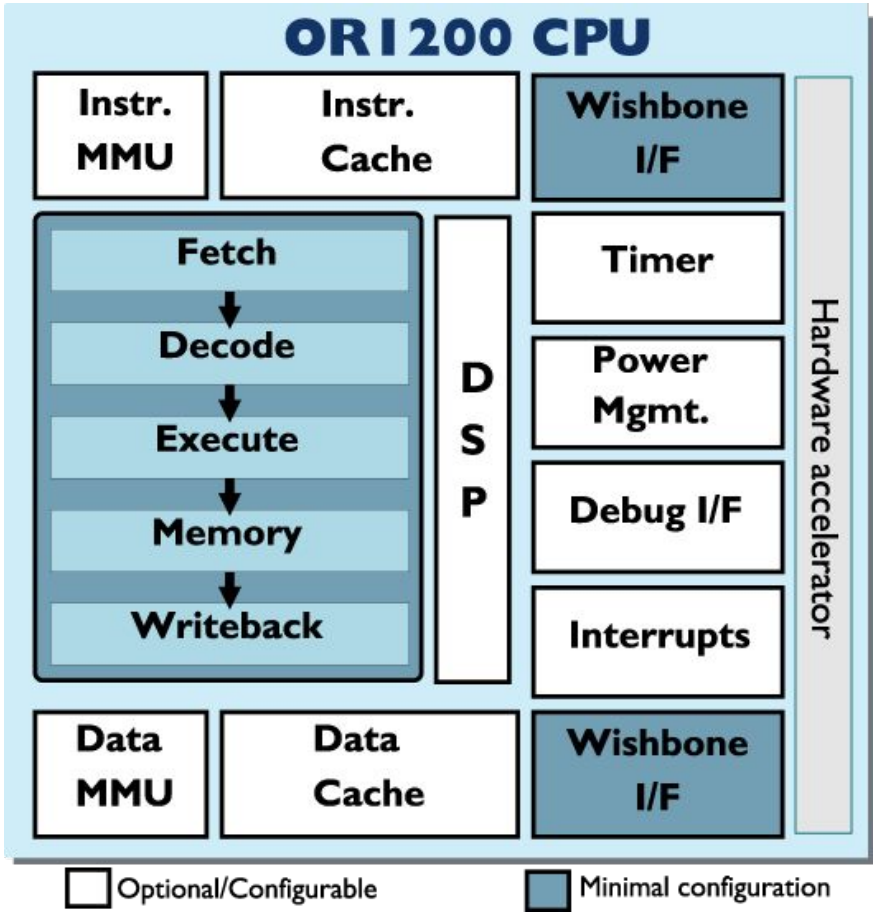
Since 2012

ORConf ➤ OpenRISC Project Conference

What is OpenRISC?

Officially OpenRISC 1000 is an open source RISC architecture:

- 32-bit ~~/ 64-bit~~
- 32 General Purpose Registers
- Delay Slot
- Instruction & Data MMU
- Linux support since 2010
  - 50mhz, 5 secs
- Open Implementations: mor1kx, or1200, marocchino

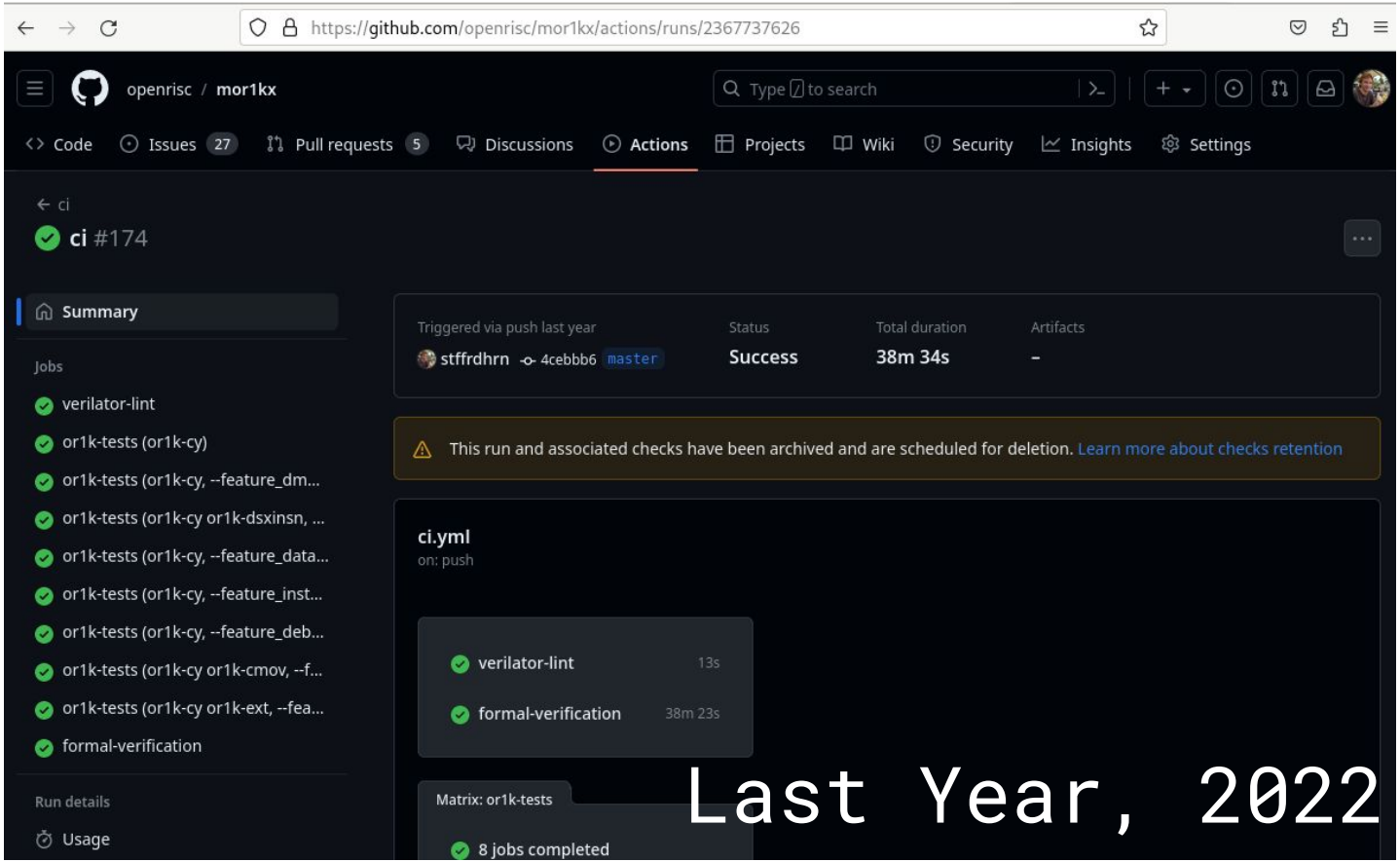


Read More: https://raw.githubusercontent.com/openrisc/doc/master/openrisc-arch-1.1-rev0.pdf

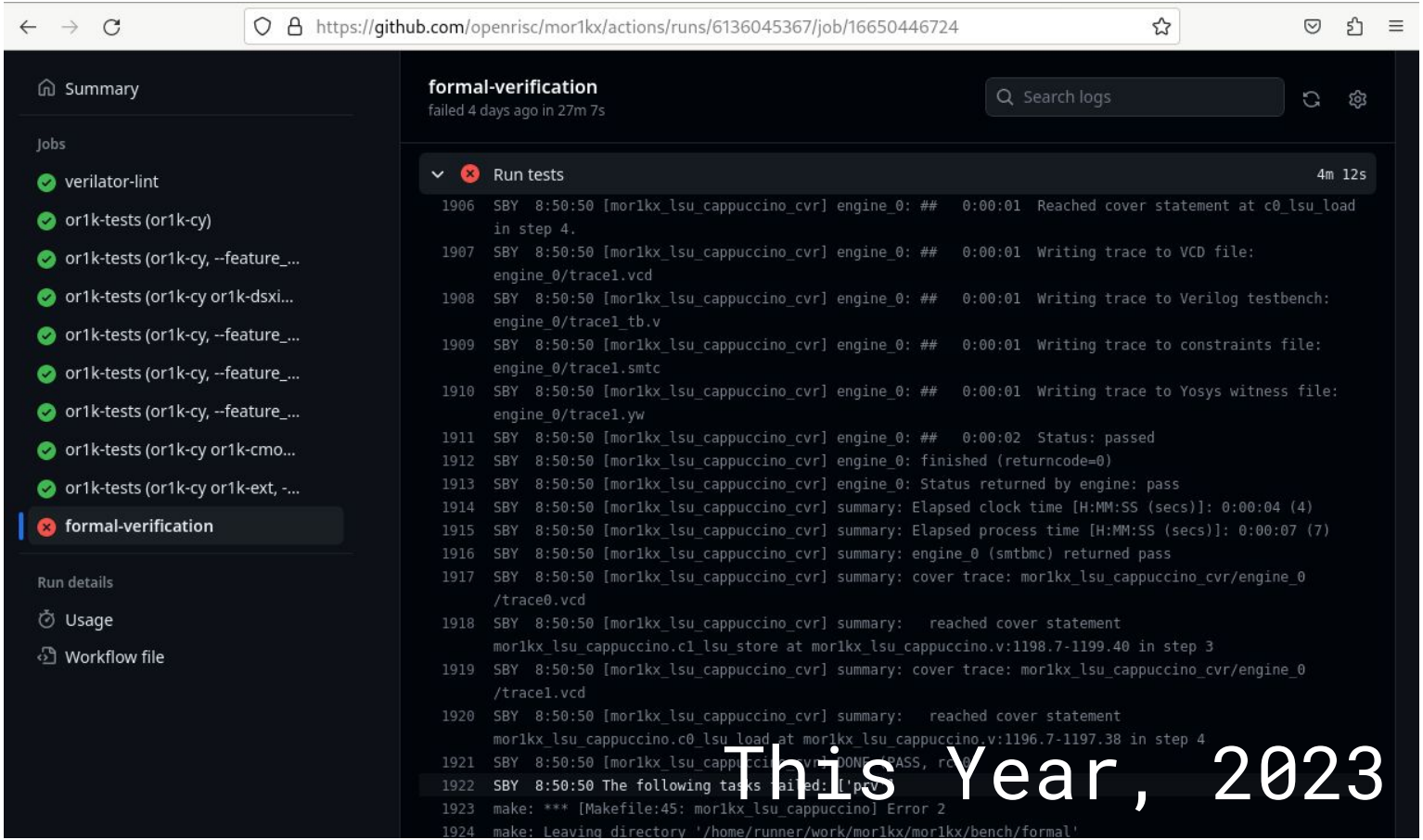

Gigi
MAJORETTES
FLIPPER
FLIPPER
MAJORETTES


OpenRISC
Linux
Simulators
Compilers
Runtime
Hardware

Mor1kx - Formal Verification

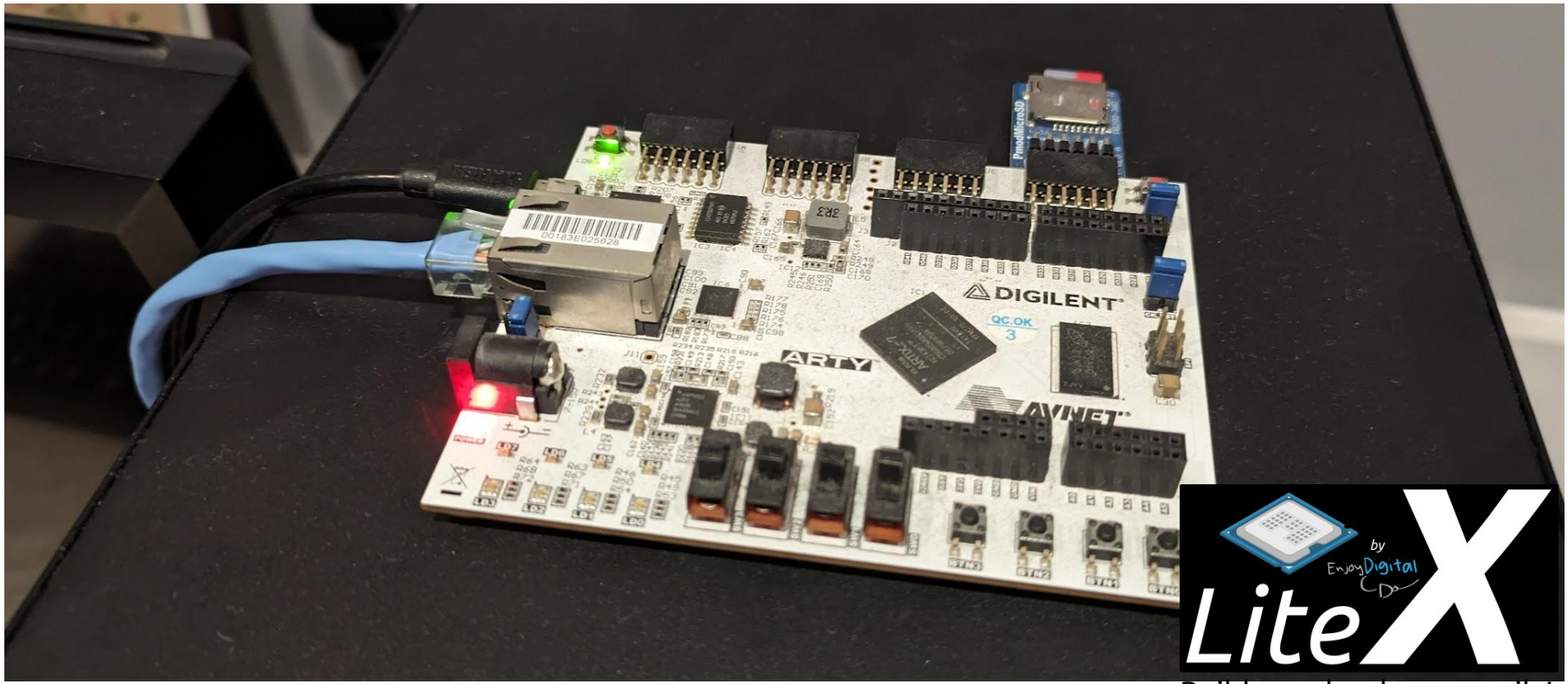


Mor1kx - Formal Verification



This Year, 2023

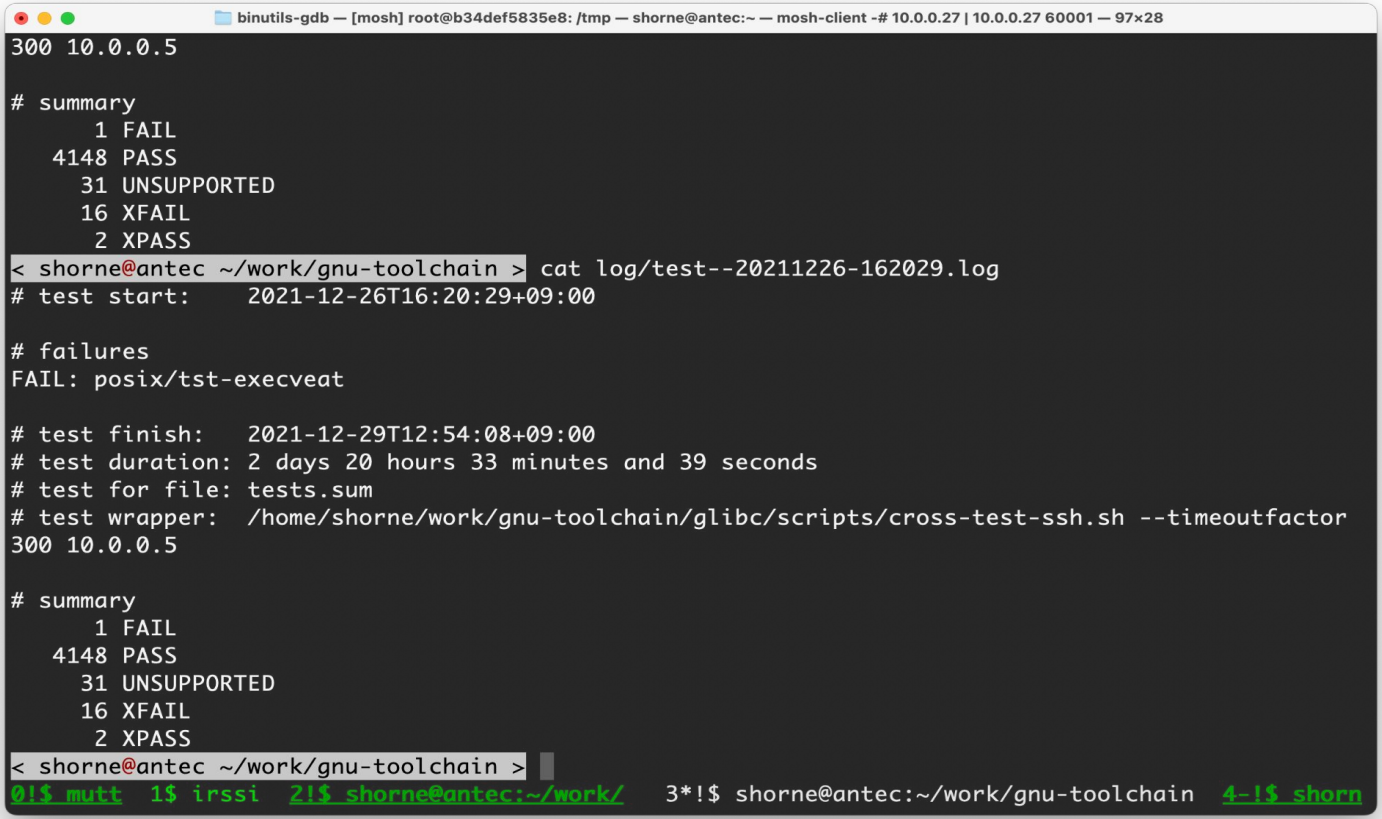
GLIBC OpenRISC Port



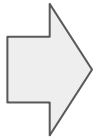
LiteX by EnjoyDigital

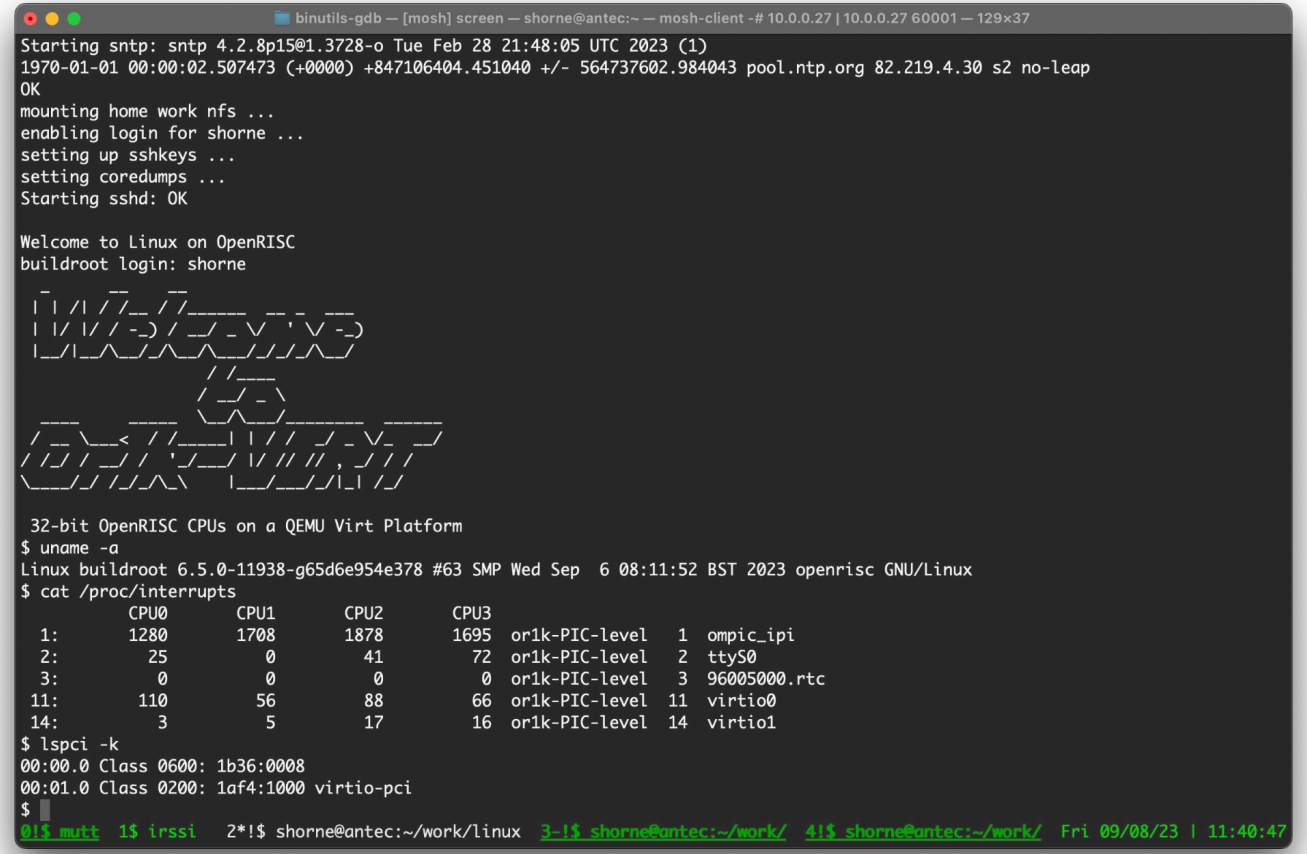
Build your hardware, easily!

GLIBC OpenRISC Port

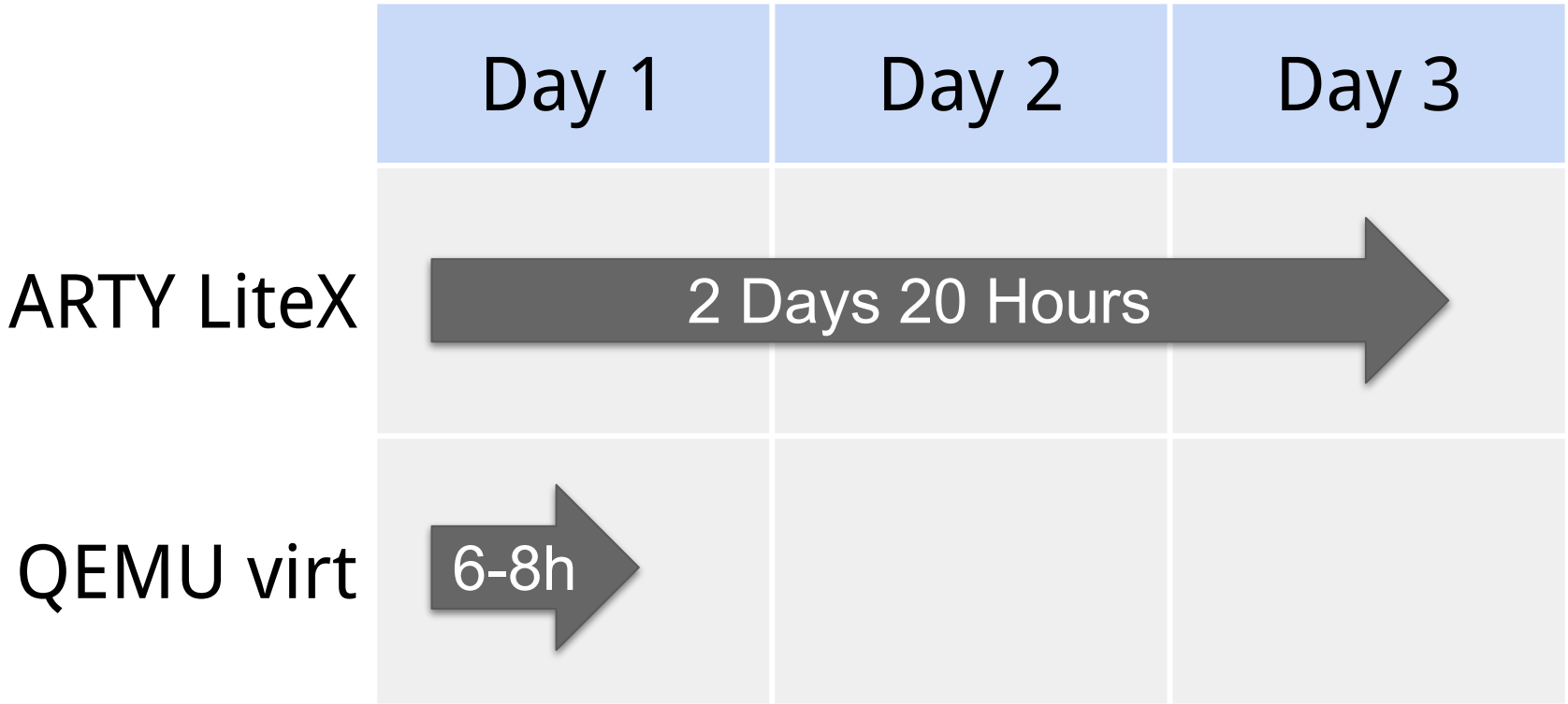


What's New - QEMU virt and PCI





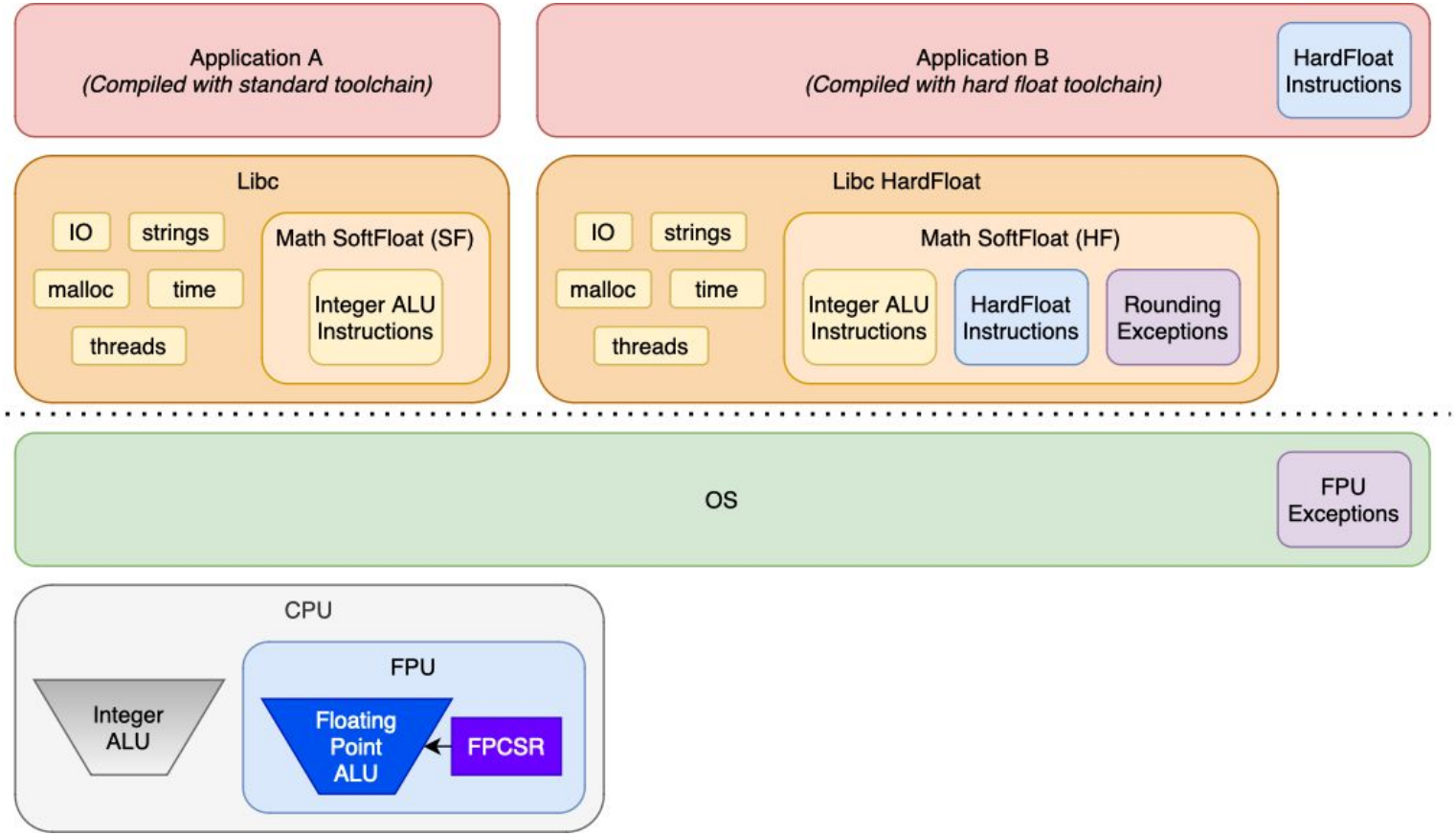
GLIBC Test Run Times



What's New

- Formal verification of mor1kx using **yosys**
- **GLibc** port upstreamed
- **QEMU** virt platform 4 cores
- PCI support added
- Mailing List moved from librecores.org to **linux-openrisc@vger.kernel.org**
- **Or1ksim** fixups and container images
- OpenRISC **specification** update 1.4

What's coming up - FPU Port



What’s coming up!

- Glibc FPU Support Upstreaming
- Improve Formal Verification
  - OpenRISC Formal
- Continued Improvements

Stafford Horne

- Open source developer since University
- OpenRISC since 2015
- Maintainer of OpenRISC ports for everything!
- Two Kids


Google Street View
Jul 2022
See more dates
新丸ビル
SHIN-MARUNOUCHI BUILDING
SMBC日興証券
SMBC NIKKO SECURITIES INC.
301
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Interested in OpenRISC?


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