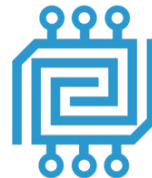


OpenRISC Update

What Happened?

Stafford Horne



ORConf 2023

What is ORConf?

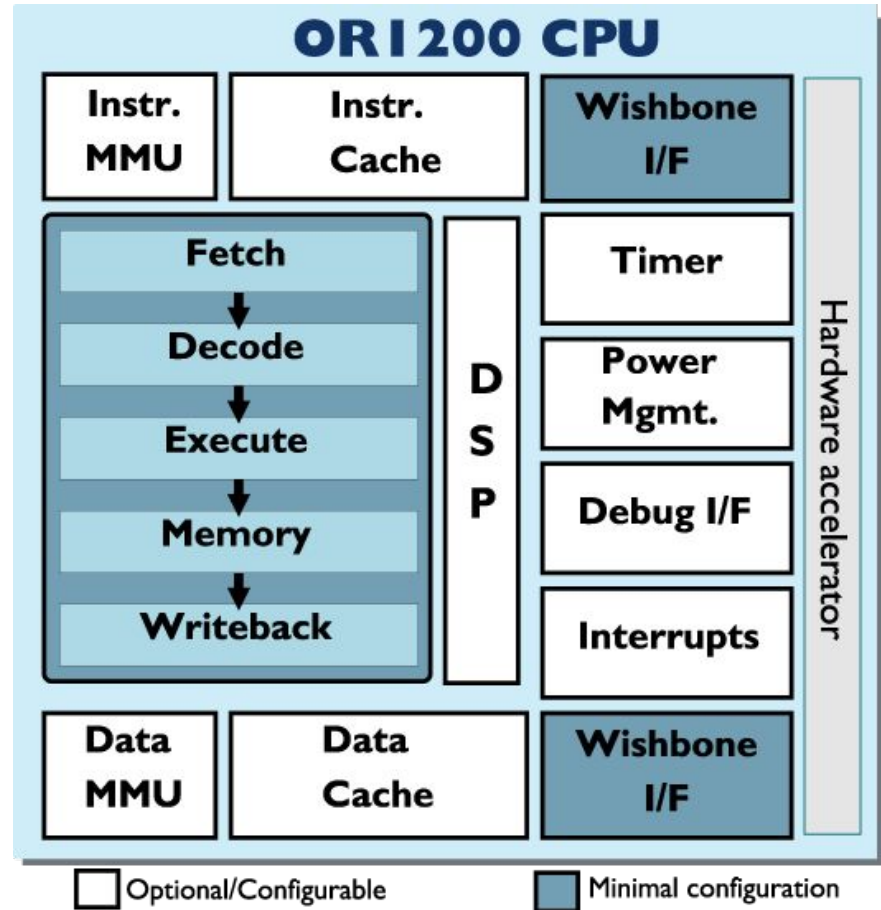
Since 2012

ORConf ➤ OpenRISC Project Conference

What is OpenRISC?

Officially OpenRISC 1000 is an open source RISC architecture:

- 32-bit / ~~64-bit~~
- 32 General Purpose Registers
- Delay Slot
- Instruction & Data MMU
- Linux support since 2010
 - 50mhz, 5 secs
- Open Implementations: mor1kx, or1200, marocchino



Read More: <https://raw.githubusercontent.com/openrisc/doc/master/openrisc-arch-1.1-rev0.pdf>





OpenRISC

Linux

Simulators

Compilers

Runtime

Hardware

Mor1kx - Formal Verification

The screenshot shows a GitHub Actions workflow run for the repository `openisc / mor1kx`. The workflow is named `ci` and the specific run is `ci #174`. The run status is **Success**. The workflow was triggered via a push last year. The total duration of the run was 38m 34s. The workflow consists of several jobs, including `verilator-lint` and `or1k-tests`. The `ci.yml` file is shown, indicating it is triggered on push. The workflow matrix is `or1k-tests`, and 8 jobs were completed.

openisc / mor1kx

Type to search

<> Code Issues 27 Pull requests 5 Discussions Actions Projects Wiki Security Insights Settings

< ci

✓ ci #174

Summary

Jobs

- ✓ verilator-lint
- ✓ or1k-tests (or1k-cy)
- ✓ or1k-tests (or1k-cy, --feature_dm...
- ✓ or1k-tests (or1k-cy or1k-dsxinsn, ...
- ✓ or1k-tests (or1k-cy, --feature_data...
- ✓ or1k-tests (or1k-cy, --feature_inst...
- ✓ or1k-tests (or1k-cy, --feature_deb...
- ✓ or1k-tests (or1k-cy or1k-cmov, --f...
- ✓ or1k-tests (or1k-cy or1k-ext, --fea...
- ✓ formal-verification

Run details

Usage

Triggered via push last year

Status: Success

Total duration: 38m 34s

Artifacts: -

⚠ This run and associated checks have been archived and are scheduled for deletion. [Learn more about checks retention](#)

ci.yml

on: push

- ✓ verilator-lint 13s
- ✓ formal-verification 38m 23s

Matrix: or1k-tests

8 jobs completed

Last Year, 2022

Mor1kx - Formal Verification

The screenshot shows a GitHub Actions workflow run for the Mor1kx project. The browser address bar displays the URL: <https://github.com/openrisc/mor1kx/actions/runs/6136045367/job/16650446724>. The left sidebar contains a 'Summary' section with a list of jobs: 'verilator-lint', 'or1k-tests (or1k-cy)', 'or1k-tests (or1k-cy, --feature_...)', 'or1k-tests (or1k-cy or1k-dsxi...', 'or1k-tests (or1k-cy, --feature_...', 'or1k-tests (or1k-cy, --feature_...', 'or1k-tests (or1k-cy, --feature_...', 'or1k-tests (or1k-cy or1k-cmo...', and 'or1k-tests (or1k-cy or1k-ext, -...'. The 'formal-verification' job is selected and highlighted with a red 'x' icon. Below the job list, the 'Run details' section shows 'Usage' and 'Workflow file' options. The main content area displays the 'formal-verification' job details, indicating it 'failed 4 days ago in 27m 7s'. A search bar labeled 'Search logs' is present. The log output shows a series of messages from 'engine_0' with timestamps '8:50:50'. The messages include: 'Reached cover statement at c0_lsu_load in step 4.', 'Writing trace to VCD file: engine_0/trace1.vcd', 'Writing trace to Verilog testbench: engine_0/trace1_tb.v', 'Writing trace to constraints file: engine_0/trace1.smtc', 'Writing trace to Yosys witness file: engine_0/trace1.yw', 'Status: passed', 'finished (returncode=0)', 'Status returned by engine: pass', 'Elapsed clock time [H:MM:SS (secs)]: 0:00:04 (4)', 'Elapsed process time [H:MM:SS (secs)]: 0:00:07 (7)', 'engine_0 (smtbmc) returned pass', 'cover trace: mor1kx_lsu_cappuccino_cvr/engine_0/trace0.vcd', 'reached cover statement mor1kx_lsu_cappuccino.c1_lsu_store at mor1kx_lsu_cappuccino.v:1198.7-1199.40 in step 3', 'cover trace: mor1kx_lsu_cappuccino_cvr/engine_0/trace1.vcd', 'reached cover statement mor1kx_lsu_cappuccino.c0_lsu_load at mor1kx_lsu_cappuccino.v:1196.7-1197.38 in step 4', 'DONE PASS, re', and 'The following tasks failed: [1]'. The log ends with 'make: *** [Makefile:45: mor1kx_lsu_cappuccino] Error 2' and 'make: Leaving directory \"/home/runner/work/mor1kx/mor1kx/bench/formal\"'.

formal-verification
failed 4 days ago in 27m 7s

Search logs

Run tests 4m 12s

1906 SBY 8:50:50 [mor1kx_lsu_cappuccino_cvr] engine_0: ## 0:00:01 Reached cover statement at c0_lsu_load in step 4.

1907 SBY 8:50:50 [mor1kx_lsu_cappuccino_cvr] engine_0: ## 0:00:01 Writing trace to VCD file: engine_0/trace1.vcd

1908 SBY 8:50:50 [mor1kx_lsu_cappuccino_cvr] engine_0: ## 0:00:01 Writing trace to Verilog testbench: engine_0/trace1_tb.v

1909 SBY 8:50:50 [mor1kx_lsu_cappuccino_cvr] engine_0: ## 0:00:01 Writing trace to constraints file: engine_0/trace1.smtc

1910 SBY 8:50:50 [mor1kx_lsu_cappuccino_cvr] engine_0: ## 0:00:01 Writing trace to Yosys witness file: engine_0/trace1.yw

1911 SBY 8:50:50 [mor1kx_lsu_cappuccino_cvr] engine_0: ## 0:00:02 Status: passed

1912 SBY 8:50:50 [mor1kx_lsu_cappuccino_cvr] engine_0: finished (returncode=0)

1913 SBY 8:50:50 [mor1kx_lsu_cappuccino_cvr] engine_0: Status returned by engine: pass

1914 SBY 8:50:50 [mor1kx_lsu_cappuccino_cvr] summary: Elapsed clock time [H:MM:SS (secs)]: 0:00:04 (4)

1915 SBY 8:50:50 [mor1kx_lsu_cappuccino_cvr] summary: Elapsed process time [H:MM:SS (secs)]: 0:00:07 (7)

1916 SBY 8:50:50 [mor1kx_lsu_cappuccino_cvr] summary: engine_0 (smtbmc) returned pass

1917 SBY 8:50:50 [mor1kx_lsu_cappuccino_cvr] summary: cover trace: mor1kx_lsu_cappuccino_cvr/engine_0/trace0.vcd

1918 SBY 8:50:50 [mor1kx_lsu_cappuccino_cvr] summary: reached cover statement mor1kx_lsu_cappuccino.c1_lsu_store at mor1kx_lsu_cappuccino.v:1198.7-1199.40 in step 3

1919 SBY 8:50:50 [mor1kx_lsu_cappuccino_cvr] summary: cover trace: mor1kx_lsu_cappuccino_cvr/engine_0/trace1.vcd

1920 SBY 8:50:50 [mor1kx_lsu_cappuccino_cvr] summary: reached cover statement mor1kx_lsu_cappuccino.c0_lsu_load at mor1kx_lsu_cappuccino.v:1196.7-1197.38 in step 4

1921 SBY 8:50:50 [mor1kx_lsu_cappuccino_cvr] summary: DONE PASS, re

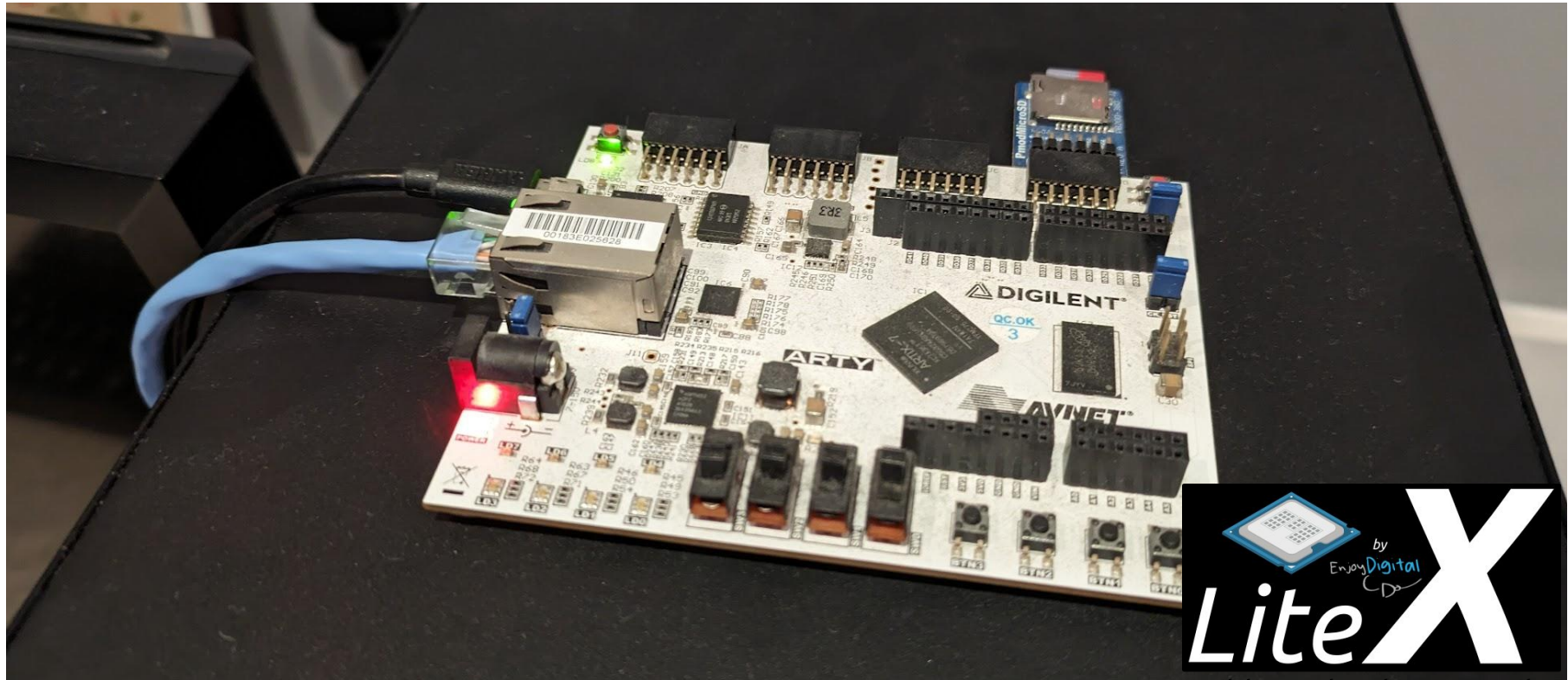
1922 SBY 8:50:50 The following tasks failed: [1]pro

1923 make: *** [Makefile:45: mor1kx_lsu_cappuccino] Error 2

1924 make: Leaving directory '/home/runner/work/mor1kx/mor1kx/bench/formal'

This Year, 2023

GLIBC OpenRISC Port



by
Enjoy Digital
LiteX
Build your hardware, easily!

GLIBC OpenRISC Port

```
binutils-gdb — [mosh] root@b34def5835e8: /tmp — shorne@antec:~ — mosh-client -# 10.0.0.27 | 10.0.0.27 60001 — 97x28
300 10.0.0.5

# summary
    1 FAIL
  4148 PASS
    31 UNSUPPORTED
    16 XFAIL
     2 XPASS
< shorne@antec ~/work/gnu-toolchain > cat log/test--20211226-162029.log
# test start:    2021-12-26T16:20:29+09:00

# failures
FAIL: posix/tst-execveat

# test finish:   2021-12-29T12:54:08+09:00
# test duration: 2 days 20 hours 33 minutes and 39 seconds
# test for file: tests.sum
# test wrapper:  /home/shorne/work/gnu-toolchain/glibc/scripts/cross-test-ssh.sh --timeoutfactor
300 10.0.0.5

# summary
    1 FAIL
  4148 PASS
    31 UNSUPPORTED
    16 XFAIL
     2 XPASS
< shorne@antec ~/work/gnu-toolchain >
0!$ mutt 1$ irssi 2!$ shorne@antec:~/work/ 3*!$ shorne@antec:~/work/gnu-toolchain 4-!$ shorn
```

What's New - QEMU virt and PCI



```
binutils-gdb — [mosh] screen — shorne@antec:~ — mosh-client -# 10.0.0.27 | 10.0.0.27 60001 — 129x37
Starting sntp: sntp 4.2.8p15@1.3728-o Tue Feb 28 21:48:05 UTC 2023 (1)
1970-01-01 00:00:02.507473 (+0000) +847106404.451040 +/- 564737602.984043 pool.ntp.org 82.219.4.30 s2 no-leap
OK
mounting home work nfs ...
enabling login for shorne ...
setting up sshkeys ...
setting coredumps ...
Starting sshd: OK

Welcome to Linux on OpenRISC
buildroot login: shorne

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32-bit OpenRISC CPUs on a QEMU Virt Platform
$ uname -a
Linux buildroot 6.5.0-11938-g65d6e954e378 #63 SMP Wed Sep  6 08:11:52 BST 2023 openrisc GNU/Linux
$ cat /proc/interrupts

```

	CPU0	CPU1	CPU2	CPU3		
1:	1280	1708	1878	1695	or1k-PIC-level	1 ompic_ipi
2:	25	0	41	72	or1k-PIC-level	2 ttyS0
3:	0	0	0	0	or1k-PIC-level	3 96005000.rtc
11:	110	56	88	66	or1k-PIC-level	11 virtio0
14:	3	5	17	16	or1k-PIC-level	14 virtio1

```
$ lspci -k
00:00.0 Class 0600: 1b36:0008
00:01.0 Class 0200: 1af4:1000 virtio-pci
$
01$ mutt 1$ irssi 2!$ shorne@antec:~/work/linux 3-1$ shorne@antec:~/work/ 4!$ shorne@antec:~/work/ Fri 09/08/23 | 11:40:47
```

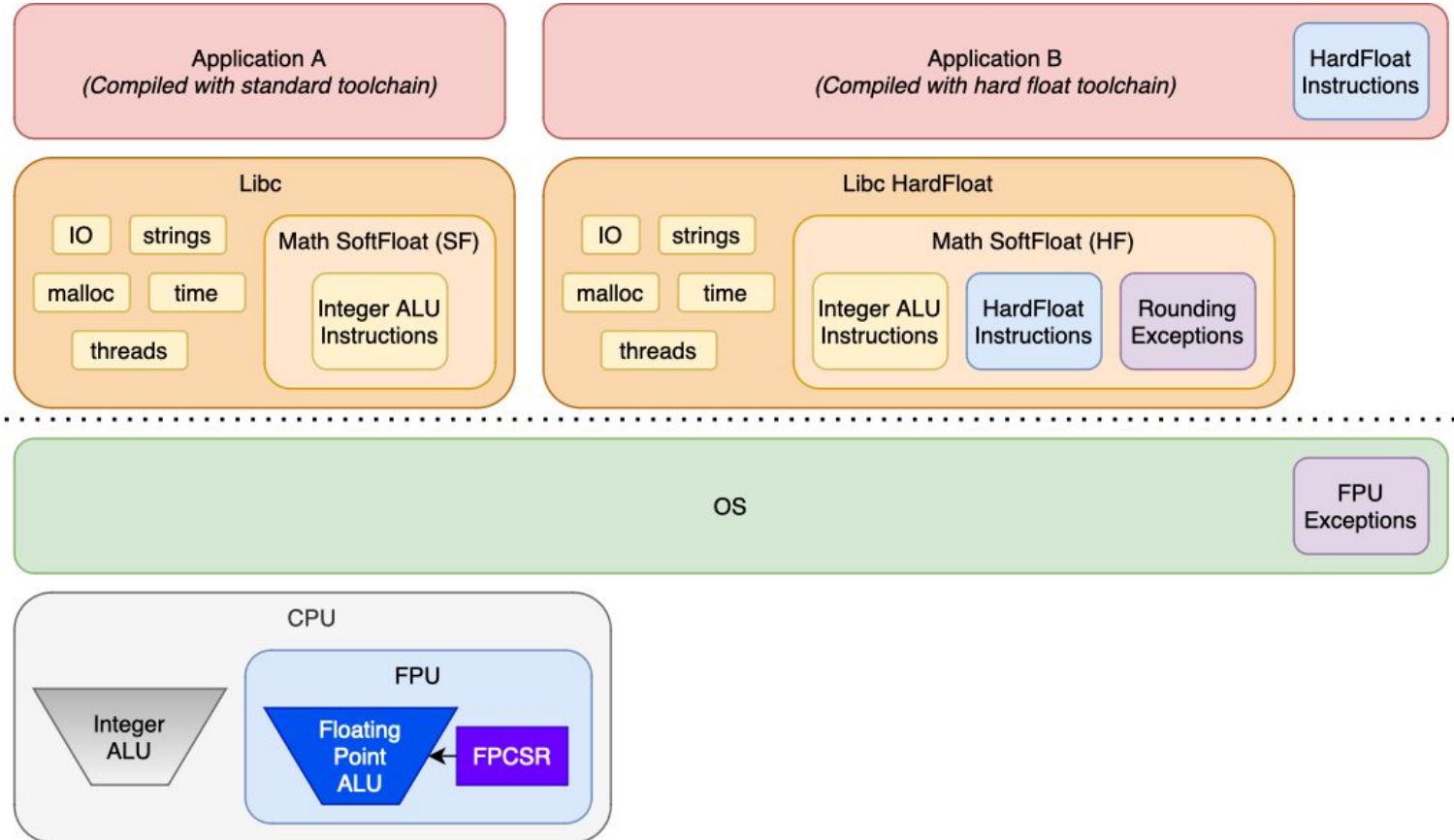
GLIBC Test Run Times

	Day 1	Day 2	Day 3
ARTY LiteX	2 Days 20 Hours		
QEMU virt	6-8h		

What's New

- Formal verification of mor1kx using **yosys**
- **GLibc** port upstreamed
- **QEMU** virt platform 4 cores
- PCI support added
- Mailing List moved from librecores.org to **linux-openrisc@vger.kernel.org**
- **Or1ksim** fixups and container images
- OpenRISC **specification** update 1.4

What's coming up - FPU Port



What's coming up!

- Glibc FPU Support Upstreaming
- Improve Formal Verification
 - OpenRISC Formal
- Continued Improvements

Stafford Horne

- Open source developer since University
- OpenRISC since 2015
- Maintainer of OpenRISC ports for everything!
- Two Kids







← Office

Tokyo Station



Interested in OpenRISC?



@stffrdhrn



<https://openrisc.io>



<https://stffrdhrn.github.io>



@shorne@mastodon.social



openrisc@lists.librecores.org