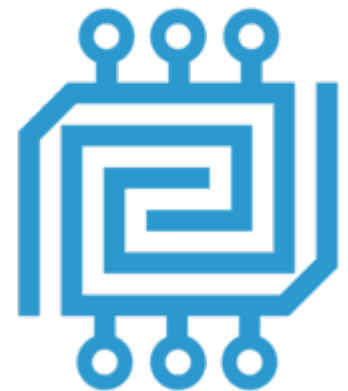




pyfda

# Python Filter Design and Analysis

Dr. Christian Münker



ORConf 2023

**Since 2008:** Professor for analog circuit design and digital signal processing at the Munich University of Applied Sciences

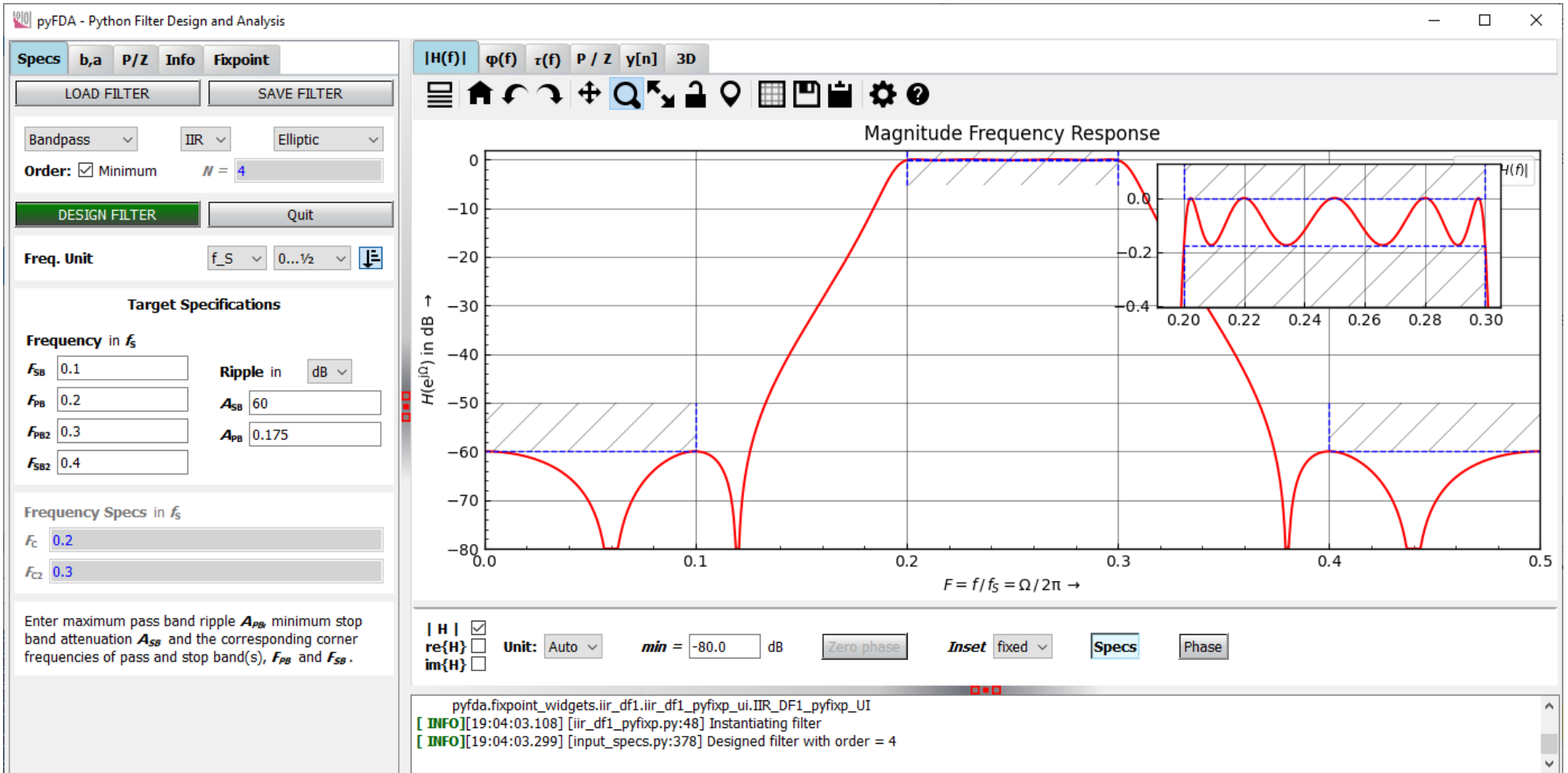
**1993 – 2008:** Mixed-signal chip designer a.o. with Infineon and Plessey



- RF-SOCs and -PLLs
- Built-In Self Test and Calibration
- Mixed-signal and behavioural simulation: SPICE, VHDL, Verilog(-A)

**Interests:** Python, DSP, FPGAs, circuit design, FOSS design flow, electronic music & music electronics, modular synths

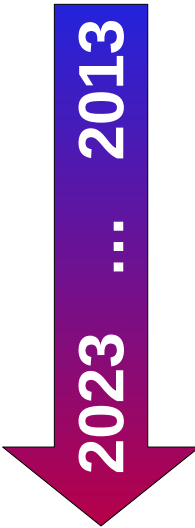
# pyfda: Python Filter Design and Analysis



[github.com/chipmuenk/pyfda](https://github.com/chipmuenk/pyfda): Self-expanding archives for Windows and OSX, flatpak for Linux or simply `pip install pyfda`



- Learn Python and QT (me)
- Interactive application for DSP lectures (me)
- Plots for lecture slides and scripts (me)
- Easy-to-use permissive license tool (DSP students, R & D)
- Fixpoint arithmetics in time and frequency domain (R & D)



## Next step

- Generate synthesizable Verilog code for fixpoint filters using e.g. amaranth

# Demo (1): Filter Design



pyFDA - Python Filter Design and Analysis

Specs | b,a | P/Z | Info | Fixpoint

LOAD FILTER | SAVE FILTER

Lowpass | IIR | Elliptic

Order:  Minimum  $N = 9$

DESIGN FILTER | Quit

Freq. Unit: kHz | 0...½

$f_s = 48$

**Target Specifications**

Frequency in kHz	Ripple in dB
$f_{PB} 10$	$A_{PB} 0.2$
$f_{SB} 12$	$A_{SB} 80$

Frequency Specs in kHz

$f_c 10$

Enter maximum pass band ripple  $A_{PB}$ , minimum stop band attenuation  $A_{SB}$  and the corresponding corner frequencies of pass and stop band(s),  $F_{PB}$  and  $F_{SB}$ .

**Magnitude Frequency Response**

$H(e^{j\Omega})$  in dB  $\rightarrow$

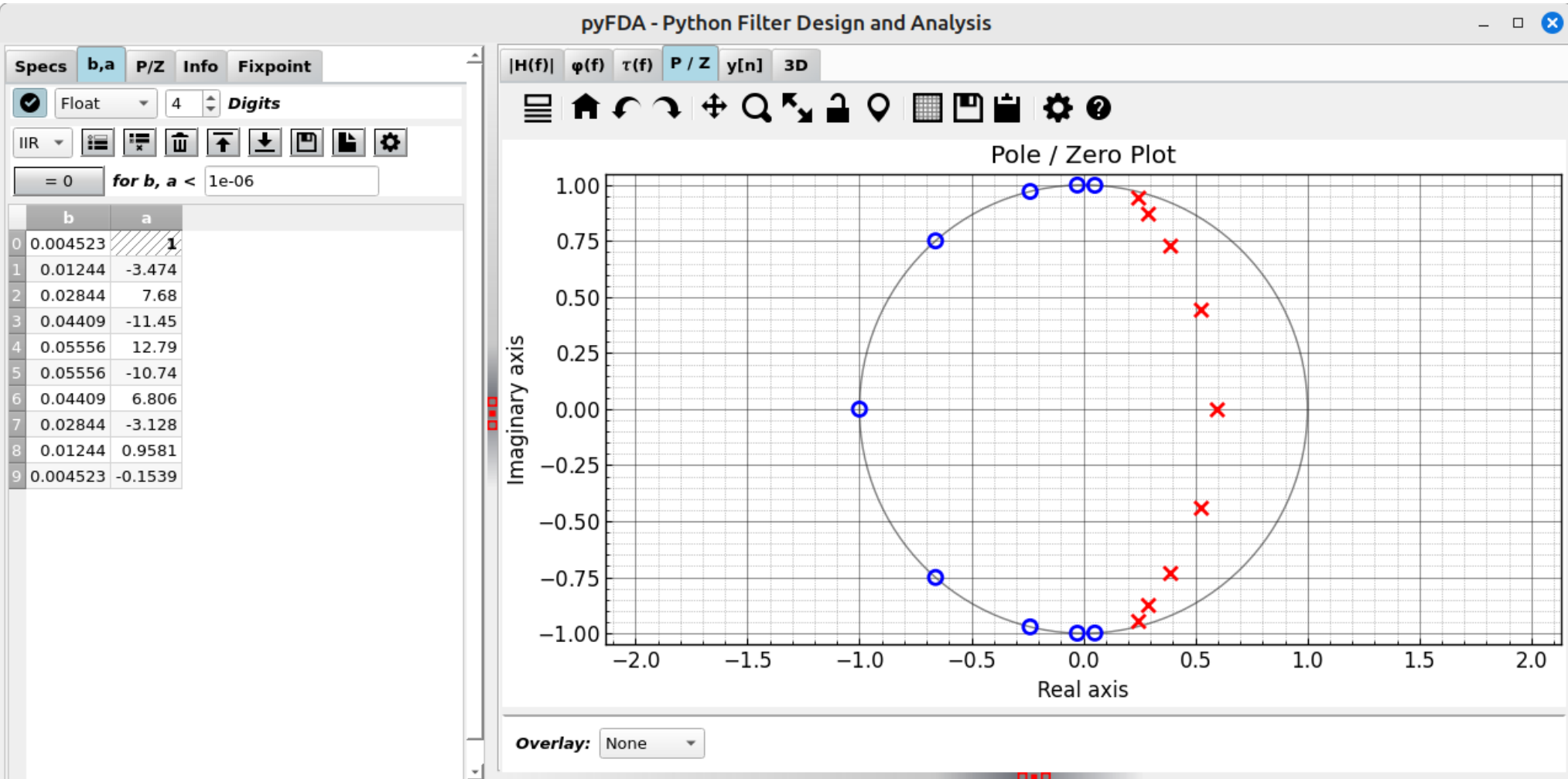
$f$  in kHz  $\rightarrow$

|H|  re{H}  im{H} Unit: Auto min = -120.0 dB Zero phase Inset edit Specs Phase

```
pyfda.fixpoint_widgets.iir_df1.iir_df1_pyfixp_ui.IIR_DF1_pyfixp_UI
[ INFO][16:43:05.812] [iir_df1_pyfixp.py:48] Instantiating filter
[ INFO][16:43:06.017] [input_specs.py:378] Designed filter with order = 9
```

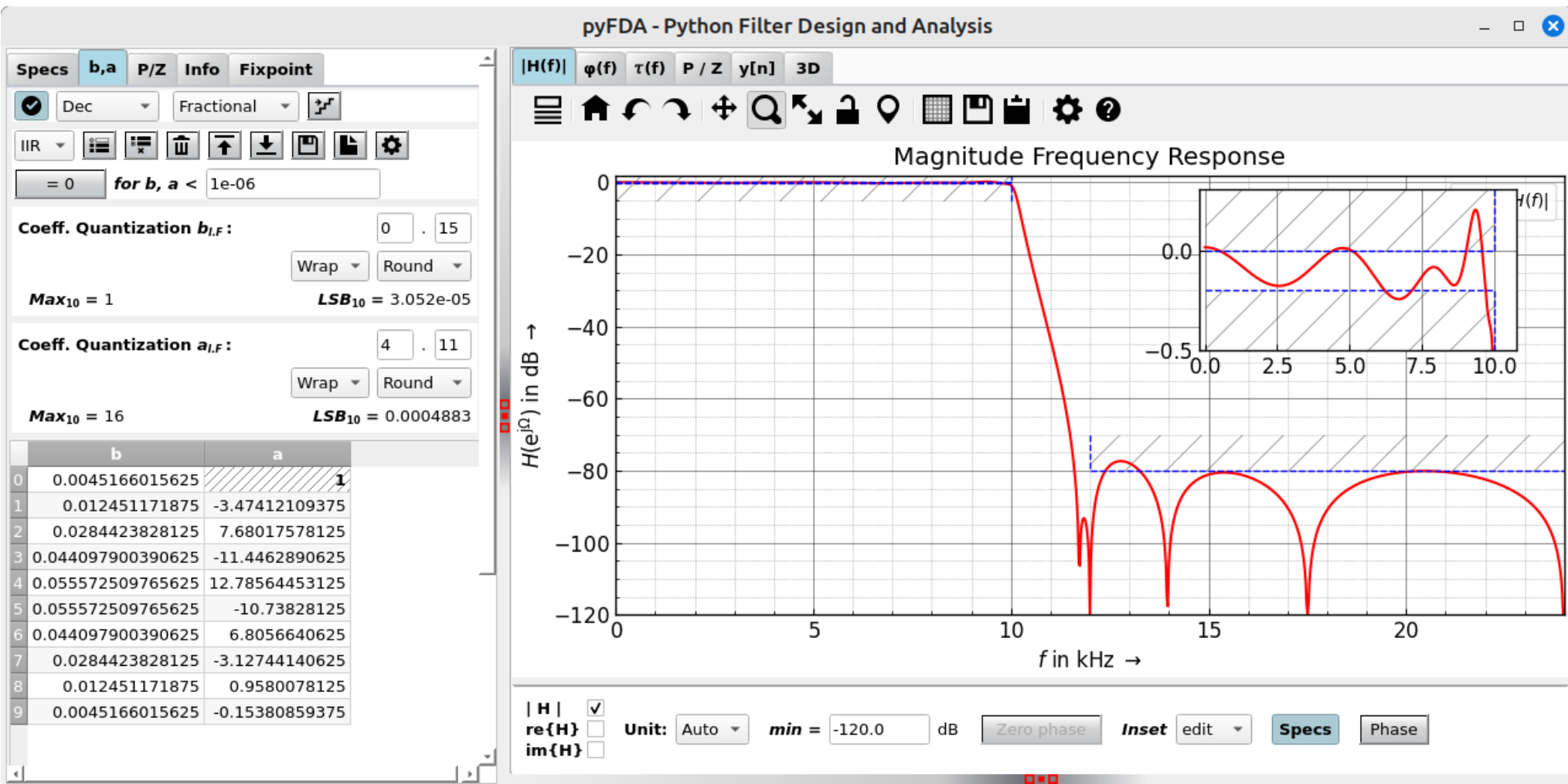
Design filter to meet frequency domain specs with minimum order

# Demo (2): Coefficients and Poles / Zeros



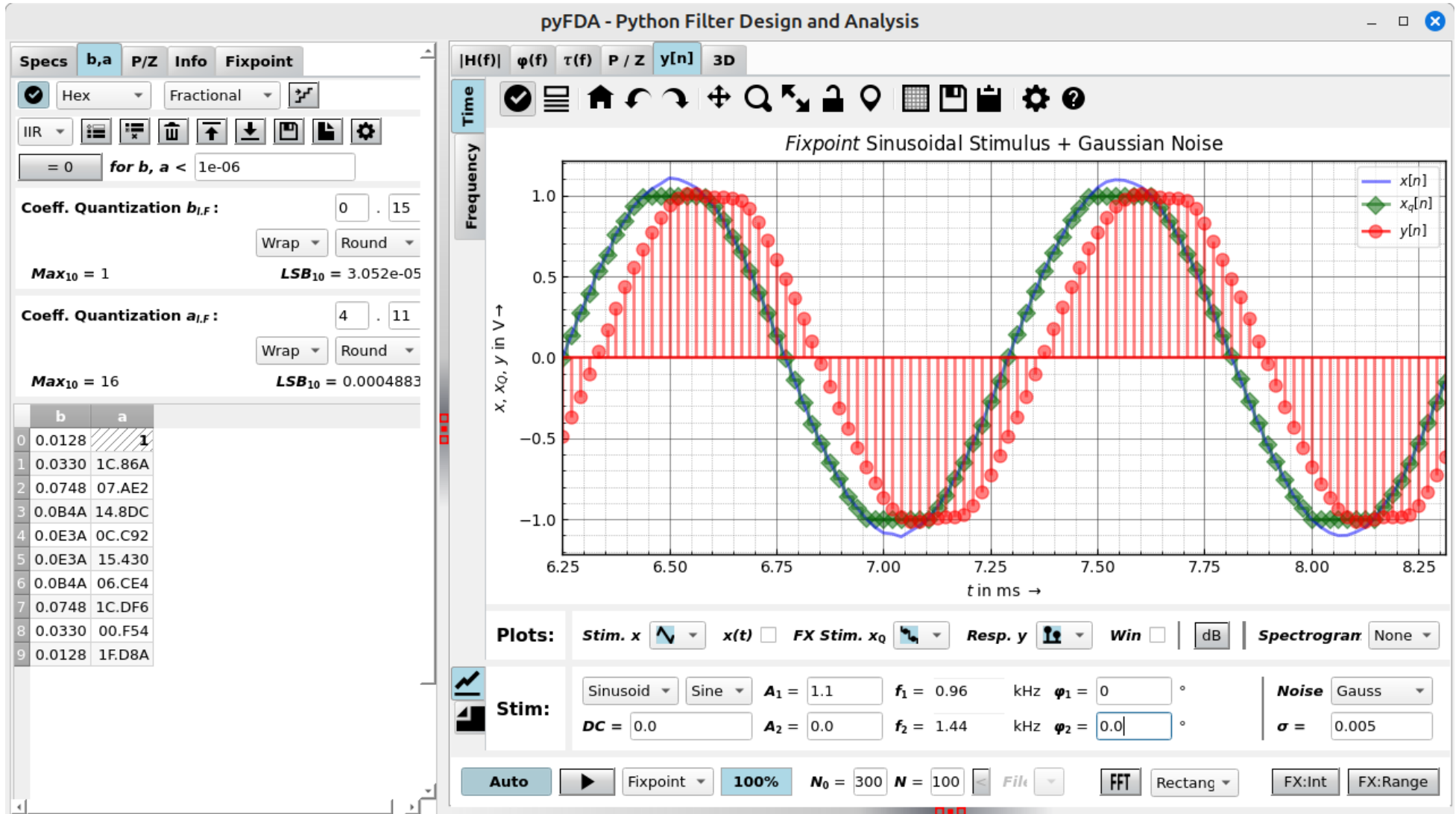
Check filter coefficients and pole / zero positions

# Demo (3): Error due to Fixpoint Coefficients



Quantize coefficients to 16 bit resolution, resulting in degraded magnitude response

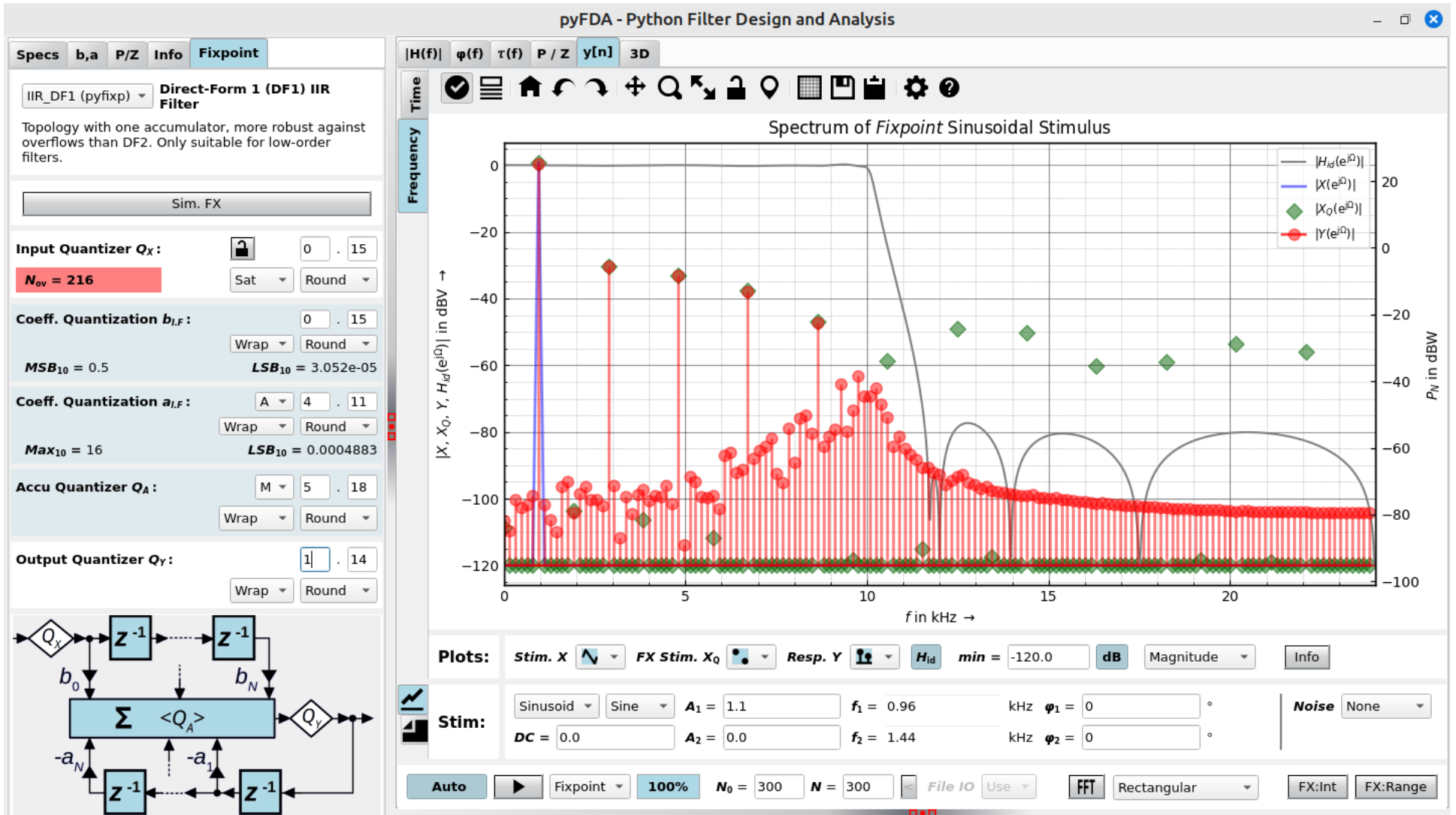
# Demo (4): Fixpoint Transient Response



View coefficients in hex format. Transient response of fixpoint filter to noisy, clipped input signal.



# Demo (5): Simulate Fixpoint Arithmetics



Spectral representation of signals from last slide together with ideal filter response



- Feedback from more R & D users, not only DSP course attendants
- Implementation of fixpoint filter topologies in a DSL (e.g. amaranth) for generation of synthesizable Verilog
- Verify generated Verilog against Python testbench using cocotb

## Contact and social media

[chipmuenk \(at\) gmail.com](mailto:chipmuenk@gmail.com)

[github.com/chipmuenk](https://github.com/chipmuenk) = [www.pyfda.org](http://www.pyfda.org)

[www.linkedin.com/in/christian-muenker](https://www.linkedin.com/in/christian-muenker)

[www.youtube.com/c/christian\\_munker](https://www.youtube.com/c/christian_munker) (tutorials coming soon)